C. Amendments to the Claims.

33. (Currently Amended) A random access memory cell, comprising:

a data storage node; and

a pass transistor coupled **to the data storage node** to provide charge transfer to and from the data storage node and including

a source region,

a drain region,

a channel region disposed between the source region and the drain region, the channel region including a first channel side and a second channel side opposite to the first channel side,

a first channel side control gate, and

a second channel side control gate wherein

the first channel side control gate is formed in a trench.

34. (Previously Presented) The random access memory cell of claim 33, further including:

a substrate insulator layer providing electrical isolation between the first channel side control gate and a substrate.

35. (Previously Presented) The random access memory cell of claim 33, further including:

a first channel side gate insulating layer disposed between the first channel side control gate and the first channel side.

36. (Previously Presented) The random access memory cell of claim 35, wherein:

the first channel side gate insulating layer include thermally grown silicon dioxide.

37. (Previously Presented) The random access memory cell of claim 33, wherein:

the first channel side control gate includes doped polysilicon.

38. (Previously Presented) The random access memory cell of claim 33, wherein:

a second channel side gate insulating layer disposed between the second channel side control gate and the second channel side.

39. (Previously Presented) The random access memory cell of claim 38, wherein:

the second channel side gate insulating layer include thermally grown silicon dioxide.

40. (Previously Presented) The random access memory cell of claim 33, wherein:

the data storage node includes polysilicon.

41. (Currently Amended) The random access memory cell of claim 33, wherein:

the first channel side **control** gate and the second channel **control** side gate are electrically connected to a word line; and

the word line is electrically connected to a word line driver.

42. (Previously Presented) The random access memory cell of claim 33, wherein:

the data storage node is a first terminal of a storage capacitor.

43. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor includes a capacitor dielectric layer including nitride.

44. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor includes a capacitor dielectric layer including Si_3N_4.

45. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor includes a capacitor dielectric layer including Ta_2O_5.

46. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor includes a capacitor dielectric layer including $SrTiO_3$.

47. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor includes a capacitor dielectric layer including $BaSrTiO_3$.

48. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor includes a second terminal shared with at least another storage capacitor of another random access memory cell.

49. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor is a trench capacitor.

50. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor has a capacitor-over-bit line structure.

51. (Previously Presented) The random access memory cell of claim 42, wherein:

the storage capacitor has a capacitor-under-bit line structure.

52. (Previously Presented) The random access memory cell of claim 33, wherein:

the pass transistor is coupled to provide charge transfer between the storage node and a bit line; and

the bit line includes metal from the group consisting of Ti, Al, and Cu.

53. (Currently Amended) The random access memory cell of claim ~~33~~ 34, wherein:

the trench is at least partially defined by the substrate insulator layer.